IN THE CLAIMS:

Please cancel claims 1-7 without prejudice, and amend the claims as follows:

1.   (Canceled)   A device, comprising:

N I/O lines, wherein N is an integer;

N internal networks;

N internal multiplexers for routing signals from individual I/O lines to individual internal networks in response to control signals; and

a multiplex controller for producing said control signals.

2.   (Canceled)   A device according to claim 1, wherein at least one multiplexer is an N-to-1 multiplexer.

3.   (Canceled)   A device according to claim 1, wherein at least one multiplexer is a 2-to-1 multiplexer.   .

4.   (Canceled)   A device according to claim 1, wherein at least one multiplexer is a 3-to-1 multiplexer.

5.   (Canceled)   A device according to claim 1, wherein at least one multiplexer can route signals to and from N-1 multiplexers.

6.   (Canceled)   A device according to claim 5, wherein each multiplexer can route signals to an associated array.

7.   (Canceled)   A device according to claim 1, wherein a multiplexer shifts signals on an I/O line to an adjacent multiplexer.

8.   (Currently Amended)   A memory device, comprising:

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N I/O lines, wherein N is [[an]] a positive integer;

N addressable arrays;

N multiplexers for selectively routing signals between said N from individual I/O lines to and said addressable arrays, wherein each multiplexer routes data between an associated array and a particular I/O line selected in response to a set of one or more control signals; and

a multiplex controller for producing said set of one or more control signals, in response to a signal provided by a device external to the memory device.

9.   (Original)   A memory device according to claim 8, wherein at least one multiplexer is an N-to-1 multiplexer.

10.   (Original)   A memory device according to claim 8, wherein at least one multiplexer is a 2-to-1 multiplexer.

11.   (Original)   A memory device according to claim 8, wherein at least one multiplexer is a 3-to-1 multiplexer.

12.   (Original)   A memory device according to claim 8, wherein at least one multiplexer can route signals to and from N-1 multiplexers.

13.   (Original)   A memory device according to claim 12, wherein each multiplexer can route signals to an associated array.

14.   (Original)   A memory device according to claim 8, wherein a multiplexer shifts signals on an I/O line to an adjacent multiplexer.

15.   (Currently Amended)   A computer system, comprising:
        a processor having at least W I/O lines;
        a bus for transferring at least W I/O bits to and from said processor;

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a memory module attached to said bus, said memory module for storing and saving a W-bit wide word, wherein said W-bit wide word is applied to said bus, wherein said memory module is comprised of a plurality of memory devices having more than W I/O lines, wherein at least one memory device has a spare I/O line that is not connected to said bus, and wherein said at least one memory device includes:

said spare I/O line;

N-1 I/O lines, wherein N is an integer;

N addressable arrays, at least one of which is associated with said spare I/O line;

N multiplexers for routing signals from said N-1 I/O lines and from said spare I/O line to said addressable arrays in response to control signals; and

a multiplex controller for producing said control signals;

wherein data on at least one of said N-1 I/O lines can be stored in and/or read from said array associated with said spare I/O line.

16.   (Original)   A computer according to claim 15, wherein at least one multiplexer is an N-to-1 multiplexer.

17.   (Original)   A computer according to claim 16, wherein at least one multiplexer is a 2-to-1 multiplexer.

18.   (Original)   A computer according to claim 17, wherein at least one multiplexer is a 3-to-1 multiplexer.

19.   (Original)   A computer according to claim 15, wherein at least one multiplexer can route signals to an associated array.

20.   (Original)   A computer according to claim 15, wherein at least one multiplexer shifts signals on an I/O line to an adjacent multiplexer.

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Please add the following new claims:

21.   (New)   A memory module for storing and saving a W-bit wide word applied to a bus, comprising:

an interface for communicating with the bus; and

a plurality of memory devices having more than W I/O lines, wherein at least one memory device has a spare I/O line that is not connected to said bus, and wherein said at least one memory device includes:

said spare I/O line;

N-1 I/O lines, wherein N is an integer;

N addressable arrays, at least one of which is associated with said spare I/O line;

N multiplexers for routing signals from said N-1 I/O lines and from said spare I/O line to said addressable arrays in response to control signals; and

a multiplex controller for producing said control signals;

wherein data on at least one of said N-1 I/O line can be stored in and/or read from said array associated with said spare I/O line.

22.   (New)   A memory module according to claim 21, wherein, within the at least one memory device:

N N-to-1 multiplexers are used;

each N-to-1 multiplexer may route data to or from any of the other N-to-1 multiplexers;

each N-to-1 multiplexer may route data to or from its associated array; and

each N-to-1 multiplexer may apply data to its associated I/O line.

23.   (New)   A memory module according to claim 21, wherein, within the at least one memory device:

2 2-to-1 multiplexers and N-2 3-to-1 multiplexers are used:

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the multiplexers are connected in series with the 3-to-1 multiplexers connected between 2-to-1 multiplexers;

 each 2-to-1 multiplexer may route data to or from its neighboring multiplexer;

 each 3-to-1 multiplexer may route data to or from any of its neighboring multiplexers;

 each multiplexer may route data to or from its associated array; and

 each multiplexer may apply data to its associated I/O line.

24. (New) A memory module according to claim 21, wherein, within the at least one memory device:

 one N-to-1 multiplexer and N-1 2-to-1 multiplexers are used;

 each 2-to-1 multiplexer may route data to and from the N-to-1 multiplexer;

 the N-to-1 multiplexer may route data to and from any 2-to-1 multiplexer;

 each multiplexer may route data to or from its associated array; and

 each multiplexer may apply data to its associated I/O line.

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